

KEYPAD/FREQUENCY SELECT BOARD 188D5771G1

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1 INTRODUCTION

The purpose of this manual is to provide service information for the Keypad and Frequency Select Board 188D5771G1. This board is used in the Orion™ and JAGUAR™ Desktop and Wall Mount Stations.

MANUAL REVISION HISTORY

REV	DATE	REASON FOR CHANGE
-	Oct. 1995	Initial release
A	Dec. 2003	Inclusion of JAGUAR data

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2 CONVENTIONS



The Note symbol calls attention to supplemental information, which may improve system performance or clarify a process or procedure.



The **ESD** symbol calls attention to procedures, practices, or the like, which could expose equipment to the effects of **Electro-Static Discharge**. Proper precautions must be taken to prevent ESD when handling circuit modules.

3 GENERAL DESCRIPTION

The primary function of the Keypad/Frequency Select Board (KFSB), 188D5771G1, is to convert the bitwise output from the DC/Tone Remote Control Boards into the proper serial data protocol. The Tone/DC Remote Control Boards 19A704686 used in the Desktop and Wall Mount Stations have bitwise inputs and outputs. This information must be integrated into the RS-485 serial control network for the station radio. The KFSB also includes an undedicated RS-232 serial port.

The KFSB reads the frequency select lines and remote PTT information from the Remote Control Board and sends it to the radio. It also controls the parallel update processes of the EDACS hardware by controlling the 2175 Hz tone generator on the 19A704686P8 EDACS® Remote Control Board. The radio does not use the station's telephone keyboard. The keyboard functions of entering LIDs and phone numbers are available by specifying the system control unit on the radio.

3.1 CONFIGURATION

Use the following information to configure the KFSB. The KFSB configuration depends on whether it is used in a conventional or EDACS remote control application. To setup the board, it will be necessary to configure R54 and select the proper serial port.

The following table summarizes the configuration information:

R54	VOLTAGE	APPLICATION
Open	5.0V	Conventional
10.0K	2.5V	EDACS

3.1.1 Configure R54

Configure R54 according to the following:

- For Conventional applications – Do Not install R54
- For EDACS applications – Install R54



NOTE

Note R54 is a critical resistor. If it is not set for the proper configuration, the KFSB will appear inactive or dead. It may also behave in a strange manner. For example, a KFSB set for conventional will not do the parallel updates of an EDACS system.

3.1.2 Select the Serial Interface

Configure the KFSB for the RS-485 driver serial interface.

Install jumpers as follows:

- P403 – Install jumper J403 on pins 2 & 3
- P404 – Install jumper J404 on pins 2 & 3
- P406 – Install jumper J406 on pins 1 & 2

A jumper on connector J406 pins 1 & 2 adds a pull-up resistor on the Service Request Line.

4 CIRCUIT DESCRIPTION

The KFSB is built around the RCP processor U1. This processor facilitates the integration of the remote control system into the network of control units. Logically, the KFSB follows the hardware arrangements. In particular, memory device addresses were fixed by the RCP. The external RAM space was set up to handle 8K or 32K devices. The application specific program code needs to reside in a flash device starting at a fixed address. This socket was laid out in a manner that can accept 128K through 512K byte devices. Flashing is handled by program code masked in the RCP's internal ROM.

An extra serial port was implemented with an ICP processor. This can be thought of more as a UART rather than a processor. It is very general purpose with programmable baud rate and data formats. Its lines are run through a MAX232 level converter IC to provide RS-232 levels at the J407 connector. Unlike a general purpose UART, the ICP contains thirty-six bits of undedicated IO plus an extra eight bit A/D. There are no connectors for this I/O. They are accessed by holes in the Board.



NOTE

The functions of the station's Remote Control Boards can be done entirely with the RCP processor. The ICP processor, the MAX232 chip, and its connectors are designed in but need not be installed.

All lines going off the board have series resistors and bypass capacitors. Additionally, 5V lines have back-to-back protection diodes. These are implemented with surface mount bridge devices. This allows one to protect two lines with one diode device. Lines that come from things touched by human hands such as the keypad and PTT lines are in particularly high need of this protection.

4.1 PROCESSOR CIRCUITY

The RCP (U1) is a sixteen bit Hitachi H8/532 microprocessor run in expanded maximum mode four with a one megabyte address space. The internal ROM is masked with an operating system and a mechanism for programming the flash PROM. The outside address space is split into places for Flash, RAM, and the ICP processor. The KFSB uses discrete circuitry to duplicate its address decoding function.

The optional ICP (U12) is an eight bit Hitachi H8/330 microprocessor run in single chip mode with its dual port RAM enabled. It can be thought of as a peripheral device of the RCP providing an auxiliary serial port and additional bitwise I/O. It is not needed for the standard remote control functions of the radio.

The flash memory (U10) needs to be above 64K (40000h and above). Its decode is done by combining A18 and A19 in OR gate U8A. This is then inverted by U2D. The output of this inverter is low if either A18 or A19 is high. The select is further qualified by AS in OR gate U8B so that it is only low on an external bus cycle. This provides the chip select to the flash memory. The processor read and write lines also go into the flash device U10.

The standard flash device is a 28F010 128K byte device. A 256K byte 28F020 may be installed with no hardware changes. An optional 5V 28F040 512K byte device may also be installed. However, resistor R16 must be removed to isolate the VPP voltage and R15 is installed to connect address line A18 to the device. Only R15 or R16 should be mounted on the Board. **Both resistors must never be installed at the same time.**

The RCP software dictates the remaining devices live in Page 0. This is when A16, A17, A18, and A19 are all low. Address lines A16 and A17 are run through OR gate U7A. Its output is low only if both inputs are low. This output of U7A then becomes one of the inputs for OR gate U7C. Addresses A18 and A19 have already been combined in OR gate U8A in order to detect the flash memory. The output of U8A is then connected to one input of OR gate U7B. U7B's second input is tied to the external address strobe line AS. This causes the output of U7B to be low only if A18 and A19 are low during an external address cycle. This output provides the second input to OR gate U7C. The output of U7C is then the Page 0 detect line. It is low only if A16, A17, A18, and A19 are all low during an external bus access cycle.

The Page 0 detect is the first part of the device decoder. The second part is provided by a pair of 74HC85 four-bit arithmetic word comparators. The "A" side of the devices is forced to 0xFA. The "B" side is connected to the upper address bus (A8 through A15). The outputs of the device with the least significant bits of the address (U6) are connected to the cascading inputs of the device with the most significant address bits (U5). The outputs of U5 then indicate if the upper byte address bits are greater than, less than, or equal to the value of 0xFA.

The positive going equal output from U5 is inverted by U2E and then combined with the Page 0 Select output line from U7C in OR gate U7D to produce the ICP select of 0x0FA00. This decode is used to talk to the ICP processor through its sixteen byte dual port RAM. The interrupt out of the ICP is brought to the RCP's IRQ0 interrupt input. The NMI interrupt on the RCP is not used and is tied to Vcc.

The greater than output from U5 is used as a select for the external RAM. It is inverted by U2F to give a zero level decode before being ORed with the Page 0 detect line from U7C in OR gate U8C. Note; a select means the address on the bus was below 0FA00. The processor's internal ROM occupies address 0x00000 through 0x07FFF. There will be no AS strobe in this address range. This effectively sets the lower limit of the RAM space to 0x8000.

The RCP software expects this RAM to start at 0x8000 and end at 0xF7FF. The Board will use a 32K device. It also has the capability of using an 8K RAM by way of series zero (0) ohm resistors on pin 26 of the RAM. For a 32K device, pin 26 is tied to A13 by zero (0) ohm resistor R17. For an 8K device, pin 26 is connected to Vcc by zero (0) ohm resistor R18. Only R17 or R18 should be mounted on the Board. **Both resistors must never be installed at the same time.**

Addresses above 0x0FA00 are not decoded. The less than output of U5 is not used. There is a selectable RAM space inside the processor from 0x0FB80 through 0X0FF7F and internal registers and ports between 0x0FF80 and 0x0FFFF. No AS strobe is generated within these address ranges.

The RCP processor runs off of 9.8304 MHz crystal X1. Balance resistor R1 and loading capacitors C3 and C4 are used to set its frequency. The micro has a pin (P10/CLK or Pin 72) provides a divide-by-two output. This output provides timing to the ICP processor. This enables the KFSB to generate the ICP's master clock without additional crystal oscillator circuit.

Most of the port pins of the RCP and ICP processors can be used as general purpose input or output bits. When used as an output, the devices have a totem pole transistor arrangement. When used as an input, a port pin will appear as a high impedance device. An open input pin will return a "0" value. Pull-ups to 5V should be used on all input lines. There are pull-up resistors on the input pins on the RCP. There are no pull-ups on the unused pins of the ICP.

The RCP's reset is provided by the reset circuit out of the L387 (U3) 5V regulator. It's duration is controlled by C6. This is also the reset line into the ICP processor. Both processor's active low standby pins are also wired high. Capacitors C5 and C7 provide filtering for the power lines.

4.2 SERIAL PORTS

The RCP processor's serial port is dedicated to providing access to the radio. Two sets of interface hardware are provided. One is a 5V open collector transistor arrangement and the other supports an RS-485 interface. The Orion and JAGUAR radios use the RS-485 configuration.

4.2.1 Open Collector Transistor Interface

The output to the radio is through Q1. 74HC04 inverter U2C compensates for the transistor's inversion. Inverter sections U2A and U2B are used to isolate the data from the radio to the processor. This interface is selected when three pin connectors J403 and J404 have jumpers on pins 1 and 2.

4.2.2 RS-485 Interface

The RS-485 interface uses a 75176 interface chip (U4). The RS-485 interface is on a single balanced line. The P17/TMO output (pin 79) from the RCP processor controls U4 through the Device Enable (DE pin 30) input. The signal is low when U4 is sending data out on the lines. The standard baud rate is 38.4K baud. This interface is selected when jumpers J403 and J404 are on pins 2 and 3.

4.2.3 Service Request Line

A third serial port control line is called Service Request Line (SRL). It is tied directly to the RCP's port pin (U1-43), allowing the software to decide if it should be an input, output, or both. The KFSB needs to be able to read and set the line, so it needs to be bi-directional. Timing of when to hold and when to release is very critical. The line also has a selectable 4.7K ohm pull-up resistor controlled by a jumper J406. Typically, this jumper is in place (J406, pins 1 & 2) to use the pull-up.

4.2.4 ASYNC Serial Port

The ICP processor can also provide a second industry standard ASYNC serial port. Its baud rate and the meaning of two handshake lines are controlled from the RCP processor. The ICP serial lines go through an RS-232 converter chip (U11) before being made available on a new board connector of J407. Its usage is not supported by standard software.

4.3 PARALLEL I/O

The KFSB also supports the Tone/DC Remote Control Boards. Up to five frequency select lines are brought on the micro Board at J402. The Control Boards use open collector transistor lines to drive these inputs. In tone applications, these lines indicate the detected function tone. Note they are also direct processor pins.

Other remote control lines go off the KFSB to the Interconnect Board via P207 or P208 before making their way to the Control Board by way of the remote interface Board. These signals include the remote PTT input and the remote channel guard input. Remote PTT can also generate an interrupt. In EDACS applications, the remote channel guard disable line is tied to the Control Board's Secur-it tone detect output. The KFSB uses this as the start of the next change function.

CIRCUIT DESCRIPTION

The Remote Boards use three open collector outputs. One, called RUS, is used to control the direction of the Remote Board's line audio drivers. It is high when the radio is unscelched. On EDACS Boards, it is also used to break the intercom loopback path during tone signaling sequences. The other two lines are called Handshake and LPTT. They are used to control the remote update hardware on the EDACS Remote Control Board. They are not needed on the conventional Remote Boards.

The KFSB makes use of station's lines brought in on P207 and P208 from the Interconnect Board. One is the Remote Off switch (REM_OFF_SW). When it is low, activity from the Remote Control Boards is basically ignored. The KFSB also has access to Desk Mic PTT and PTT. They are set as inputs, but they are not currently used. The remote transmissions are keyed either from remote PTT through logic on the Remote Interface Board or via serial messages from the KFSB. The radio arbitrates between the two PTT choices.

5 OPERATION

There are major differences between conventional and EDACS remote control operation. Remote channel guard disable in conventional is Secur-it tone detect in EDACS. There are no parallel status updates in conventional operation.

The KFSB also needs to know what type of radio is installed in the station. This is the main task of Mode Select resistor R54. It is part of a voltage divider with R9 from 5V. The divider is fed into one of the RCP's A/D inputs. The use of the divider and A/D allows for selection of many choices from one processor pin. The A/D voltage value currently determines the choice of EDACS or Conventional operation. The A/D is read only at power-up. Open and shorted conditions can also be considered "states."

5.1 REMOTE CONTROL STATION OPERATION

All remote controlled EDACS stations are equipped with Tone Remote Board 19A704686P8. This board contains the tone decode and encode (generation) circuitry necessary for EDACS remote control applications. The decode circuitry decodes the Secur-It Tone/function tone sequences originating from the EDACS Remote Controller(s).

The decoders' outputs drive the KFSB's frequency select inputs at J402. The tone encode circuitry generates 2175 Hz tone bursts used for remote handshaking and update signaling. This tone generation circuitry is directly controlled by the KFSB.

Two (2) output control lines from microprocessor U1 connect to the Tone Remote Board. These output lines control the Tone Remote Board's 2175 Hz tone generator. They are identified as LOCAL PTT (P207 pin 6) and HANDSHAKE (P207 pin 7). The HANDSHAKE line provides on/off tone control and the LOCAL PTT line provides high/Low level tone control. Pull-up resistors are located on the Tone Remote Board for the open-collector transistor inverters, Q3 and Q4.

In an EDACS station, the KFSB does not process any remote input (SF lines or PTT (FROM REMOTE) line) until it receives a Secur-It tone validation pulse on the SEC DET line (P207 pin 12). The Tone Remote Board pulls this line low when the Secur-It tone is present on the transmit phone line (line from Remote Controller). Any SF or PTT (FROM REMOTE) input changes not preceded by a SEC DET pulse are considered invalid and are ignored by the KFSB.

Immediately after the Secur-It tone is detected (SEC DET transitions low), microprocessor U1 brings LOCAL PTT and HANDSHAKE lines high. With LOCAL PTT and HANDSHAKE high, the Tone Remote Board outputs a high-level 2175 Hz handshake tone burst to the EDACS Remote Controller(s) via the receive phone line pair. This tone burst informs the initiating EDACS Remote Controller that the station received its Secur-It tone. It also informs any paralleled EDACS Remote Controller(s) that a control function is occurring from another (the initiating) EDACS Remote Controller. This temporarily prevents any paralleled remote from transmitting a Secur-It/function or Secur-it/function/hold tone sequence. The high-level 2175 Hz tone burst lasts approximately 140 milliseconds, and it is sent out at a level equal to the Secur-It tone (approximately +10 dBm). See Figure 1.

Microprocessor U1 reads the SF inputs at J402, 20-milliseconds after the Secur-It tone drops. This is exactly in the center of the 40-millisecond function tone. This ensures an accurate function tone decoder read.

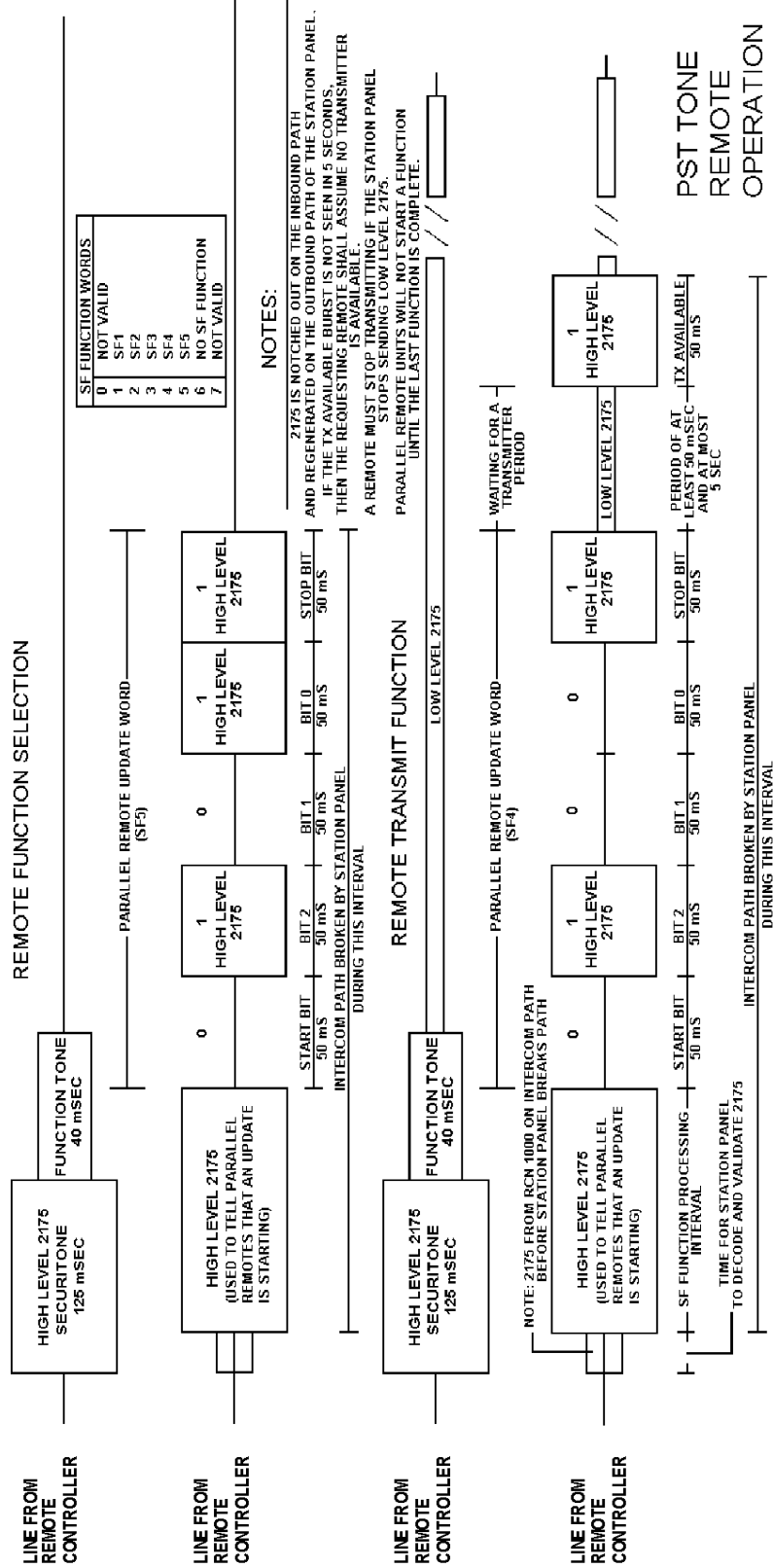


Figure 5-1: Remote Function Selection

Next, U1 starts a serial communication sequence with the radio. The function tone selection is then passed to the radio. Next, the radio checks its personality memory to see if the new SF selection information is a valid system/group. It then responds with a serial communication sequence to U1 on the KFSB.

At this point, the KFSB sends a 5-bit SF update word to the EDACS Remote Controller(s) via the receive phone line pair(s) using the 2175 Hz tone generator on the Tone Remote Board. This word updates the SF selection LED indicators at any paralleled EDACS Remote Controllers and it communicates valid/invalid SF selection (per radio SF personality programming) to the initiating EDACS Remote Controller. If the selection is not valid, the initiating remote will return to the previous SF selection and any paralleled remotes will never change their SF selections.

The 5-bit SF update word is generated by switching the 2175 Hz tone generator on the Tone Remote Board on and off. As shown in Figure 1, a logic 1 is represented by a high level 2175 Hz tone and a logic zero (0) is represented by a quiet line. Each bit period lasts 50-milliseconds.

The start bit is zero (0), three data bits follow, and the stop bit is one (1). The LOCAL PTT (P207 pin 6) and HANDSHAKE (P207 pin 7) outputs from the KFSB control the tone generator circuit on the Tone Remote Board. Both are high when a high-level 2175 Hz tone is present (logic 1) and both are low during a quiet line (logic 0) period.

The chart in Figure 1 defines the Special Function selections that the three data bits correspond to within the 5-bit update word. The left column is the octal code of the three data bits. Codes 1 through 5 correspond to the desired system/group SF selection (SF1 - SF5 respectively). Codes 0 and 7 are not valid. Figure 1 shows update sequences SF4 and SF5.

Code 6 indicates the selection does not correspond to a programmed system or group in the station's mobile radio. This can occur if the system or group is reprogrammed at the radio or if not all five (5) system/group selections are programmed into the radio. If an EDACS Remote Controller receives a code 6, it considers it as a "no valid system/group selection" and it turns off all of its SF selection LED indicators.

System/group changes or PTTs made at the EDACS station also causes the 5-bit SF update sequence to occur. It also occurs when the station is powered up.

5.2 REMOTE TRANSMIT FUNCTION

The previous circuit analysis includes information on the control signaling sequences that occur for both a remote (non-transmit) function selection and a remote transmit function. As shown in Figure 1, additional control signaling is required between the EDACS Remote Controller(s) and the station for a remote transmit function. This additional signaling is described in the following paragraphs.

As in a conventional system, the 2175 Hz transmit hold tone sent out from an EDACS Remote Controller is present on the transmit phone line (line from Remote Controller) until the PTT is unkeyed. This hold tone signals the station that the remote is keyed. During the hold tone period, Tone Remote Board I9A704686P8 pulls the PTT (FROM REMOTE) input at P207 pin 11 low. Microprocessor U1 reads this low and thus recognizes the keyed EDACS Remote Controller.

As shown in Figure 5-1, after the 5-bit SF update word is sent out, a low-level 2175 Hz tone is applied to the receive phone line pair (line to Remote Controller). This tone, generated by the Tone Remote Board, signals the EDACS Remote Controller's that the station is waiting for a channel assignment from the EDACS site. As with the initial high-level 2175 Hz handshake and the 5-bit SF update, the KFSB uses its LOCAL PTT (P207 pin 6) and HANDSHAKE (P207 pin 7) outputs to control the 2175 Hz tone generator circuit on the Tone Remote Board. LOCAL PTT is high and HANDSHAKE is low when the low-level 2175 Hz tone is present on the receive phone line pair.

Next, the initiating EDACS Remote Controller must be notified when the station receives a working channel assignment from the EDACS site. This is accomplished, as shown in Figure 1, by a 50-millisecond high-level 2175 Hz tone burst sent to the EDACS Remote Controller via the receive phone line pair. This tone burst is known as the "OK to talk" burst. HANDSHAKE switches high for 50 milliseconds to switch the tone generator on the Tone Remote Board to a high-level output.

When the initiating EDACS Remote Controller receives the "OK to talk" tone burst, it opens its microphone audio path and sounds its "OK to talk" beep. After the high-level 2175 Hz "OK to talk" burst occurs, the KFSB switches the tone generator back to a low-level for the duration of the remote key. This is accomplished by switching HANDSHAKE back to a low level and leaving LOCAL PTT high for the remainder of the key.

If the station does not receive a working channel assignment from the EDACS site within five seconds, the "OK to talk" burst will not be generated. The KFSB will re-initialize itself for another Secur-It/function/hold tone sequence.

5.3 CONVENTIONAL DESKTOP STATIONS

The KFSB monitors the five (5) SF lines and the PTT (FROM REMOTE) line at P207 pin 11 from the Conventional DC/Tone Remote Board. The SEC DET line at P207 pin 12 goes to the KFSB but is not used. The DC/Tone Remote Board pulls PTT (FROM REMOTE) low when a remote control unit signals for a station key. The SEC DET (Secur-It tone detect) line from the DC/Tone Remote Board is really a Channel Guard disable line; it does not signal the presence or absence of the Secur-It tone in a conventional tone remote controlled system.

Upon reading a change in one of the input lines, microprocessor U701 starts a serial communication sequence with the radio. This sequence transfers the new channel or function information to the mobile radio.

There is much variety in the operation of tone control systems. For example, many remote control units do not send the tone sequence for a channel change until there is a PTT. If a KFSB does not respond to a frequency change from a remote, verify the remote actually sends a tone sequence for the Board to act upon.

6 FLASHING OPERATIONS

6.1 GENERAL

The 12-volt VPP voltage for the flash comes onto the Board at P208 pin 9. This is an unused pin on the current KFSB. It is also an unused pin on the Interconnect Board. VPP is protected by a low value resistor and a 15v zener diode. If U10 is a 512k byte flash device, the 5v VPP also happens to the A18 line. A Zero ohm series resistor R15 is used to decide which signal goes to the device's pin. The RCP serial port lines on J208 can be used to tie to the flashing computer through a TQ3370 box via the J401 keypad and display serial lines. Jumpers J403 and J404 must be configured for the open collector transistor hardware (Pins 1 and 2) to bring the serial port to this connector.

The KFSB must be removed from the station to flash by J208. The reason for this is the KFSB's serial port sense is opposite that of the radio. This is a result of being able to talk to the radio. The personality/flash capabilities from the microphone connector of the station are also meant to talk to the radio. It is the same sense as the KFSB. Therefore, connecting TXD to TXD and RXD to RXD results in no communications.

Flashing can also be done by connecting a flashing cable to J408 and J401. This can be done with the KFSB mounted in the station. The VPP is on flashing connector J408 pin 6. Jumpers J403 and J404 must either be removed or in the JAGUAR/Orion position to flash from this connector. The serial lines connecting the KFSB and the computer are on J408 pins 4 and 5. Pin 2 of J408 is tied to ground in the TQ3370 box. This disables the RS-485 receiver's output, so that only the computer drivers are on the RCP's receive line.

The RCP's internal ROM software controls the flashing process. It makes assumptions about the hardware that are not valid in the KFSB. One of these is that J401 pin 5 must be high and J401-13 must be pulled low. This is accomplished with the flashing cable's J401 connector.

Another situation involves the RCP's power-up process. Part of the power-up sequence determines if there is a display or control unit connected to the KFSB. The absence of the Display or control unit creates an error condition that hangs the software in an exception handling loop. In the radio, the watchdog timer in the modem would clear this error. However, the KFSB does not contain a modem IC, hence no watchdog reset. The board will appear to die and the flash program will stop.

The solution is to manually reset the RCP. A reset after power-up is somewhat different than a reset at power-up. In this situation, the lack of a display or control head will not hang the micro. Because of this, the reset line is brought out on flashing connector J408-3. The flashing cable ties this line to the momentary PTT switch in the TQ3370 box. If the KFSB does not flash immediately after power-up, press the PTT switch and try flashing again. It may take several attempts to get the Board's attention.

An alternate method of determining if one is in flash mode is to check for a specific pattern on A0. When in flash mode, there should be address pulses for about half a millisecond every three milliseconds. Constant or no pulses on A0 indicate the Board is not in flash mode. The Board will be in program mode on every second reset.

6.2 FLASHING THE KFSB

The software in the JAGUAR 725M/M7100/Orion 188D5771 KFSB is contained in a software re-flashable memory device. An update requires a TQ3370 Interface Box, a 19B802554P27 Programming Cable, and updated flash software in a .bin file. The following programming procedure assumes that the TQ3370 Interface Box is properly connected to the computer's serial port and that the ProGrammer™ software is properly set up to program radios.

6.2.1 Hardware Setup

1. Turn the power switch on the desktop station's power supply to OFF.
2. Remove the top cover from the desktop station.
3. Remove the screws from the JAGUAR 725M/M7100/Orion radio, slide the radio backward on the supports, and lift it out. Place it to the side so there is access to the Keypad/Frequency Select board (KFSB).
4. The radio can remain attached to the Interconnect board. However, use the radio ON/OFF/Volume knob to turn the radio power OFF.
5. Connect the DB25 end of the 19B802554P27 programming cable to the "Radio" port of the TQ3370 box.
6. Connect the 6 pin connector to J408 on the KFSB board close to the standing TO220 regulator. The connector must be oriented so that pin 1 is closest to the regulator. Pin 1 is to the left when connector wires are pointed up and connector retainer lip is facing user. When installed on J408, the connector's retainer lip shall face into the interior of the KFSB board. See the diagram below.
7. Connect the 14 pin connector to J401 on the opposite side of the board as J408. The end of the connector with the wire on it must face the corner of the board so there are wires in pins 1 and 13 of the connector. The cable between the KFSB's J402 and the remote control board may be left on without affecting the flashing process. See the diagram below.
8. Now turn on the power switch on the desktop station power supply. Press the PTT Switch on the TQ3370 box once. This is necessary to force a reset that puts the KFSB board into software update mode. The board is now ready to be flashed. See the Flashing Procedure.

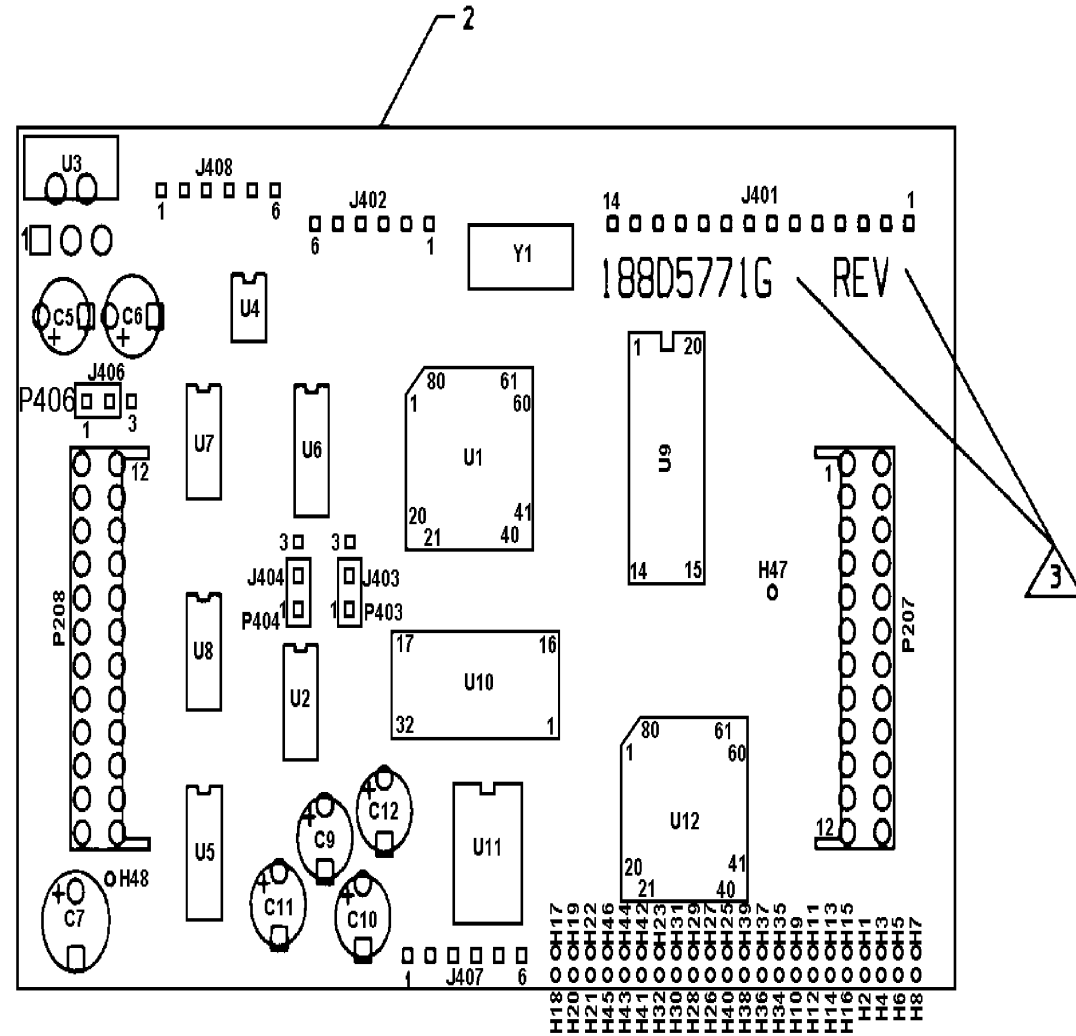
6.2.2 Flashing Procedure

1. The KFSB board flash software is updated from the Radio Maintenance program. To access the Radio Maintenance program, select Radio Maintenance from the "M/A-COM Software Tools" menu.
2. When the Radio Maintenance dialog box appears, click on the MRK/LPE/Orion/EDACS 500M/JAGUAR/P7100/M7100 tab.
3. In the MRK/LPE/Orion/EDACS 500M/JAGUAR/P7100/M7100 tab, click on the Desktop button.
4. Select the desired file to flash into the KFSB board. Click on the Open button after the file has been selected. Follow the instructions provided as the KFSB board is flashed.
5. If there is a problem, see the Troubleshooting section.

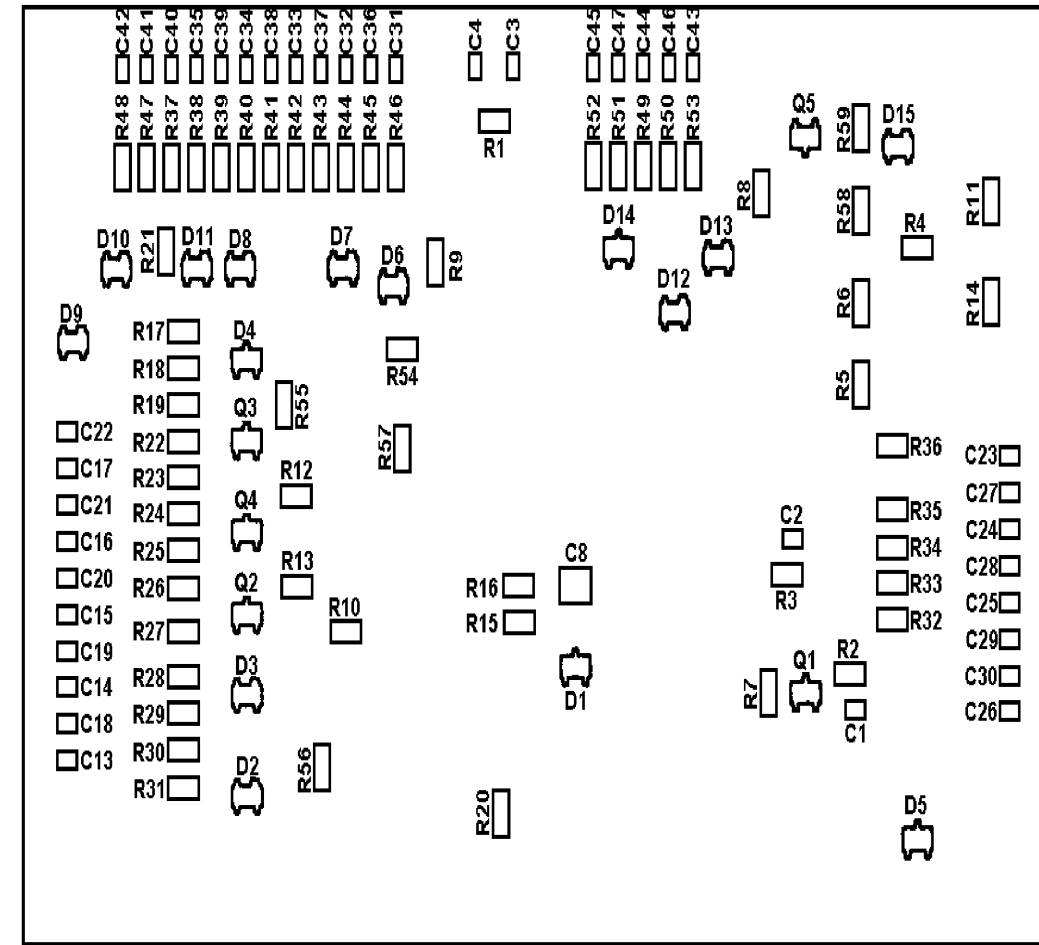
6.2.3 Troubleshooting

1. The KFSB board has a unique power up test mechanism that requires an odd number of reset pulses to force it into flash update mode. Occasionally the TQ3370 box's PTT switch may cause an even number of reset pulses and prevent the board from entering the flash update mode. If the board does not flash, it may be helpful to press the TQ3370 box's PTT switch and then rerun the flash program.
2. Occasionally the KFSB board does not recognize flash update mode even with an odd number of reset pulses. If repeated pressing of the PTT switch does not result in the flash program being accepted, power down the desktop station power supply and try again. Since there is not much of a load on the power supply, it will take several seconds before the filter capacitors in the supply discharge. Do not turn the supply back on until you here a distinctive click from the power supply.
3. Verify the JAGUAR 725M/M7100/Orion radio is turned off. If it is on, the messaging between the transceiver and the control unit will interfere with the KFSB board's flash update. If there is a concern about loading, remove the jumpers from J403 and J404 on the KFSB board. This will guarantee the serial data path between the KFSB board and the TQ-3370 box is isolated from the radio's control network.
4. It may be useful to verify the KFSB board is operating properly. This can be verified by looking at Address Line 0, on Pin 10 of the U9 static ram. When the board is operating properly, there will be a distinctive pattern of 250 microsecond bursts of activity every 2.5 seconds. Failure to see this pattern typically means the KFSB board is not in flash mode and is not operating.

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VIEW FROM COMPONENT SIDE

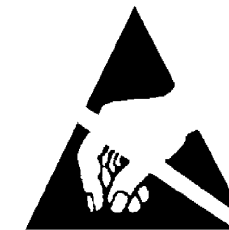


VIEW FROM SOLDER SIDE

①

NOTES:

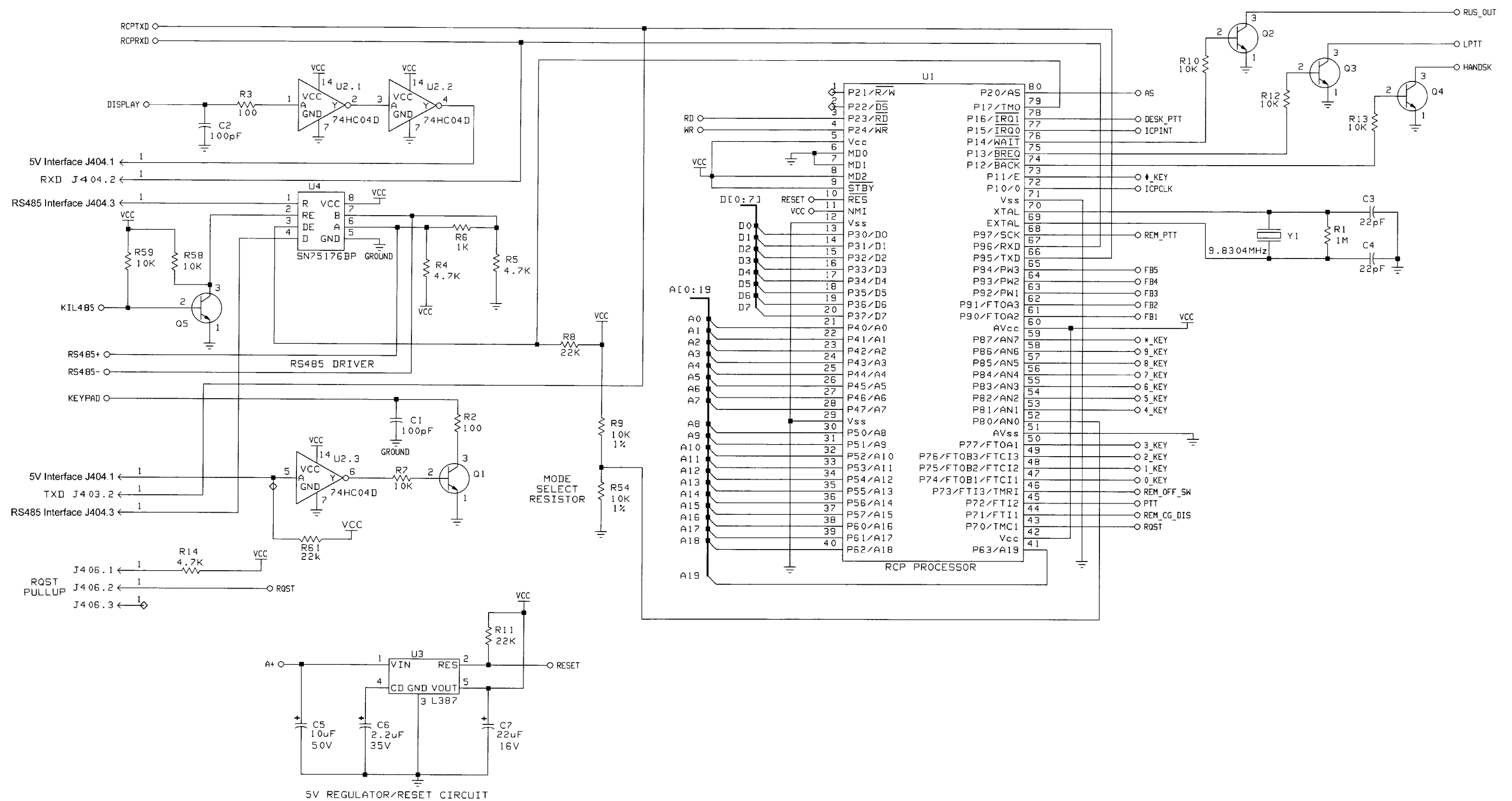
1. SOLDER ALL ELECTRICAL CONNECTIONS.
2. COMPONENT LEADS TO PROTRUDE .06 MAX. BELOW SOLDER SIDE OF BOARD.
- ③ MARK APPLICABLE GROUP NUMBER AND REVISION LETTER PER 19A115740P1 CHARACTERS .12 HIGH, COLOR BLACK FOR LATEST REVISION LETTER SEE 19C852060 INDEX



CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

KEYPAD/FREQUENCY SELECT BOARD
188D5771G1
(188D5771, Rev. 0)

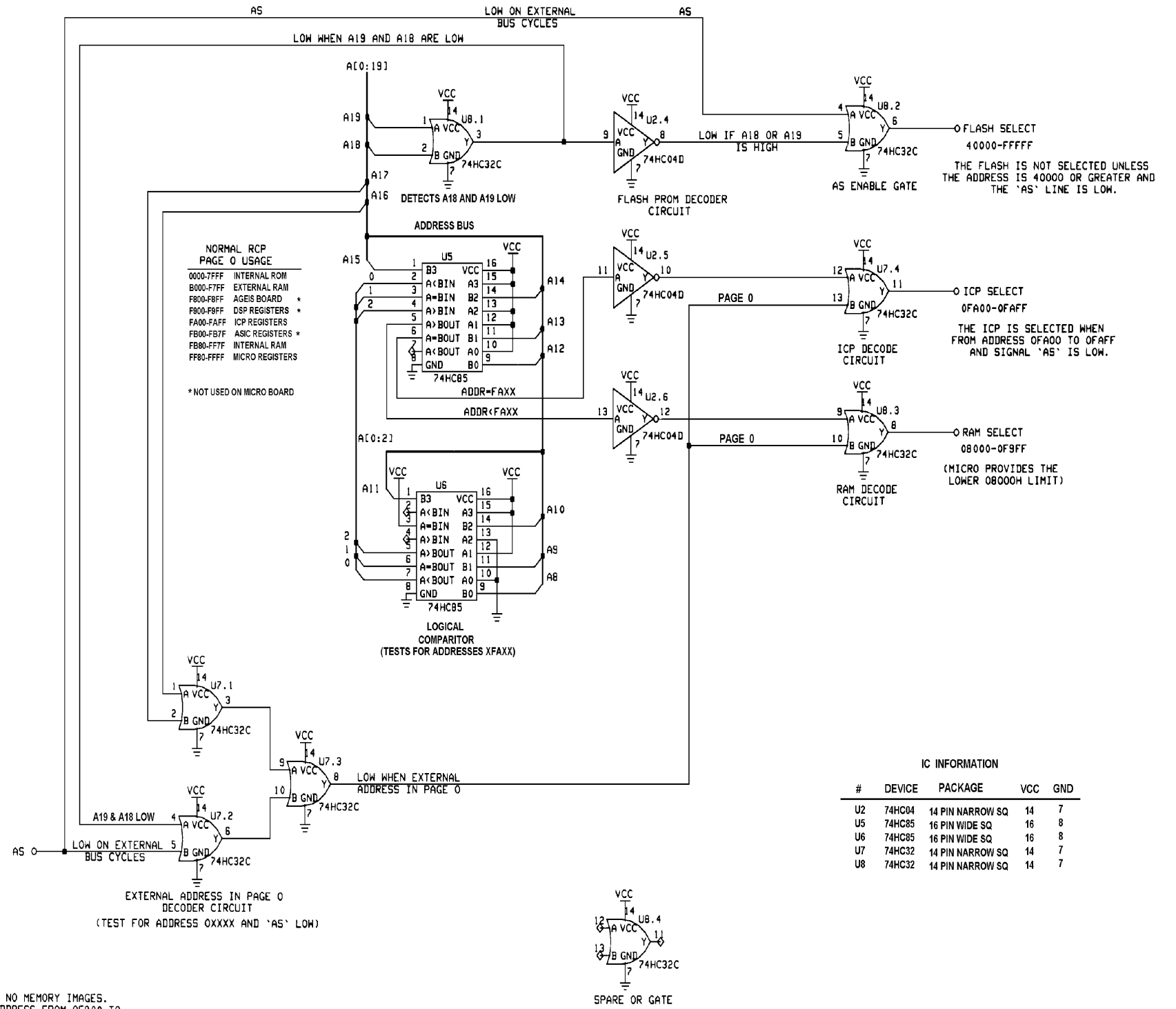
SCHEMATIC DIAGRAM



KEYPAD/FREQUENCY SELECT BOARD

188D5771G1

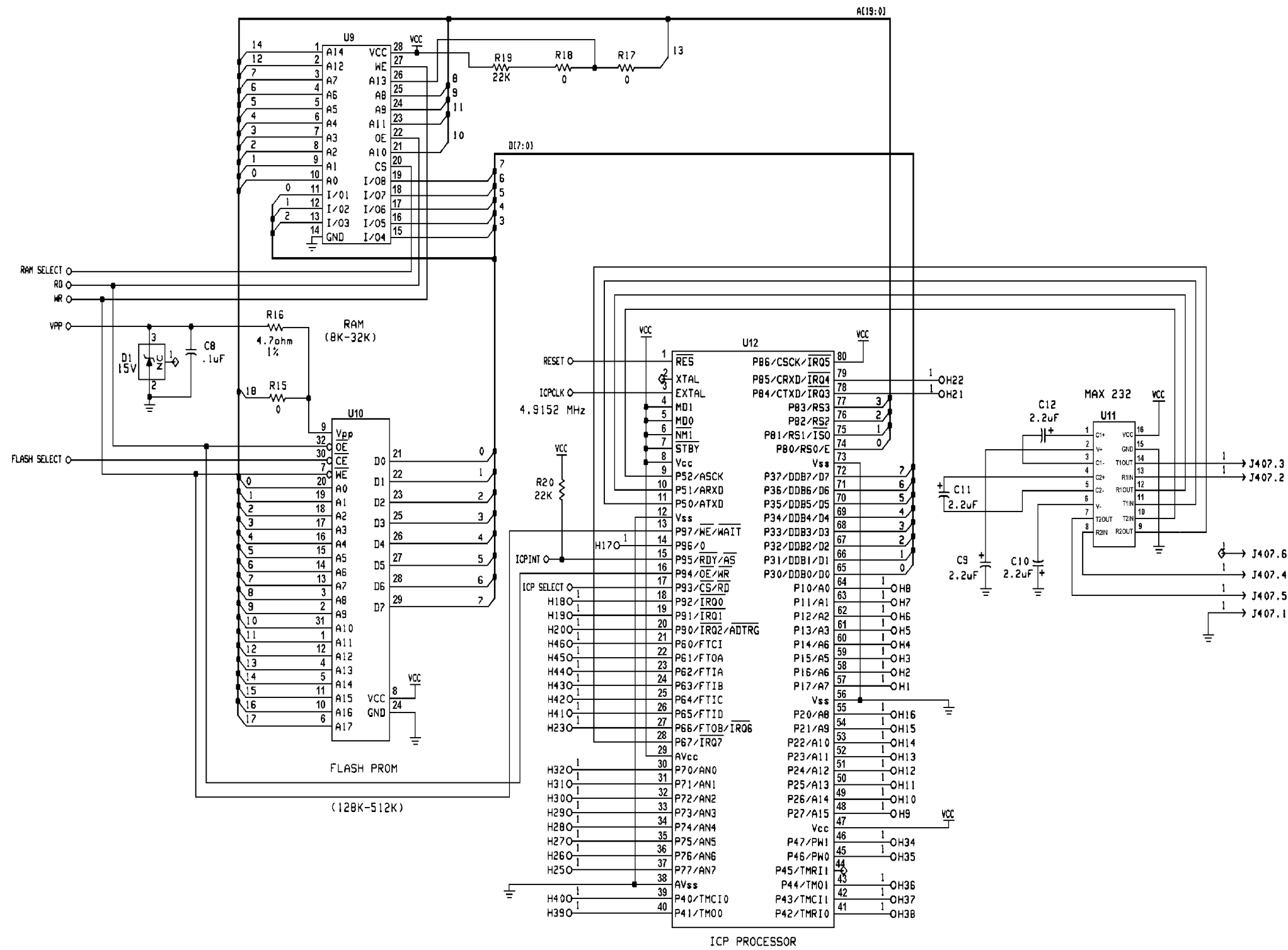
(188D5772, Sh. 2, Rev. 3)



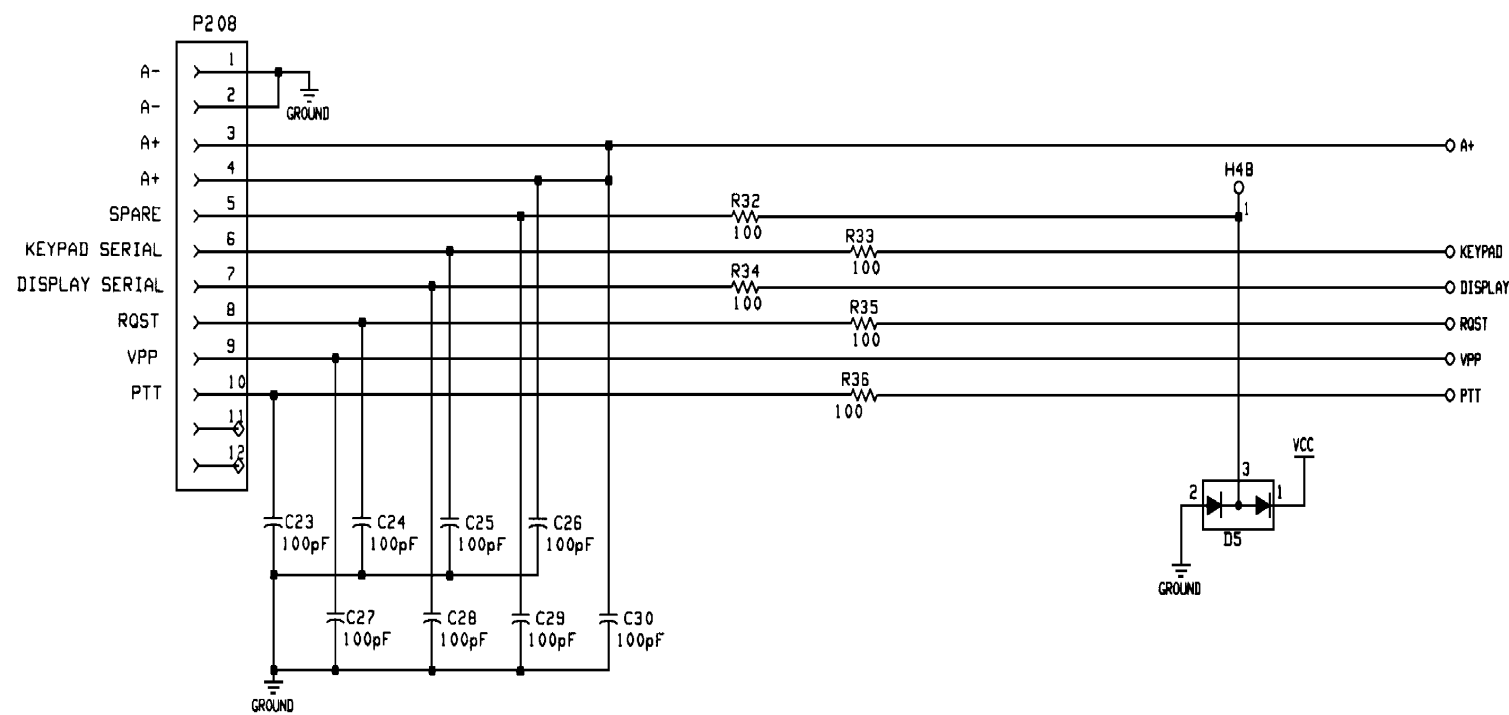
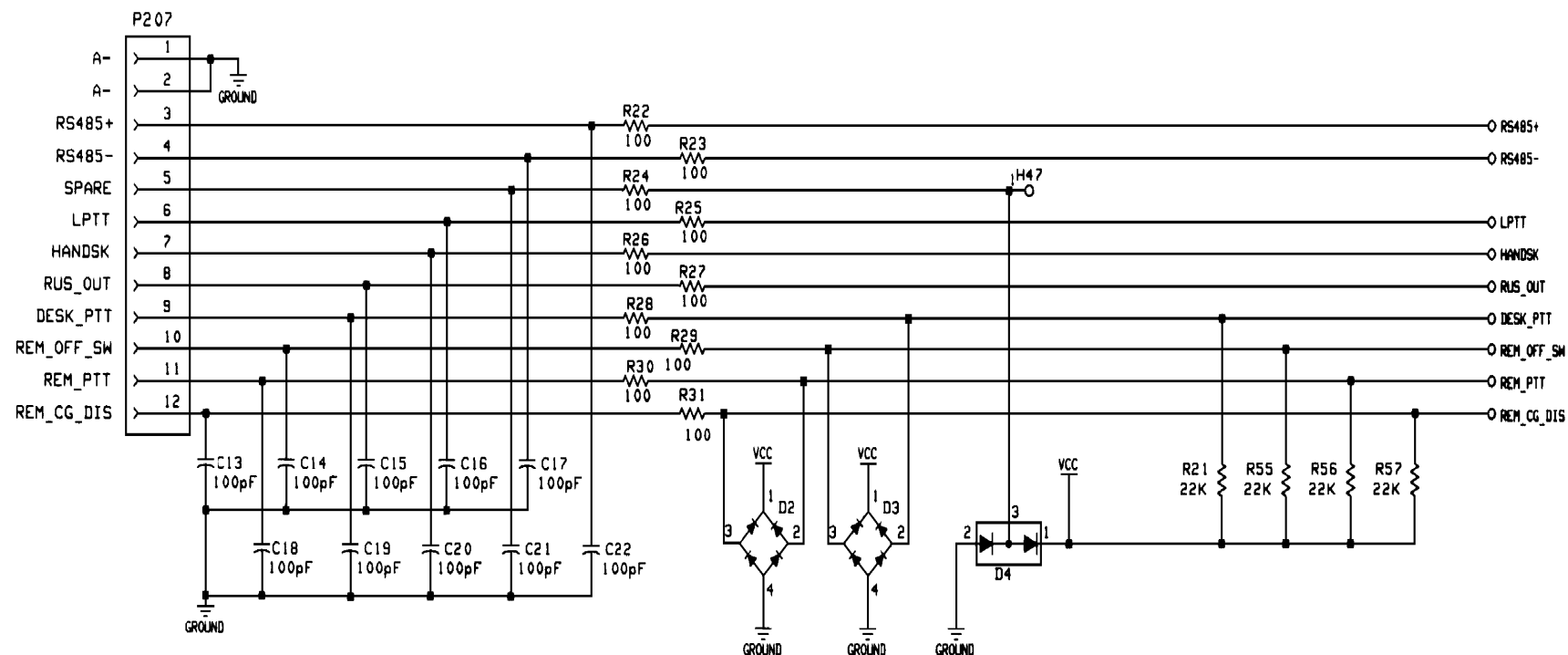
THIS APPROACH HAS NO MEMORY IMAGES. HOWEVER, DEVICE ADDRESS FROM 0F800 TO 0F9FF WILL MAP TO THE UPPER ADDRESS SPACE OF THE RAM. ALL DEVICES ARE ALSO UNSELECTED UNLESS IN A BUS CYCLE. (SIGNAL 'AS' LOW)

**KEYPAD/FREQUENCY SELECT BOARD
188D5771G1
(188D5772, Sh. 3, Rev. 1)**

SCHEMATIC DIAGRAM



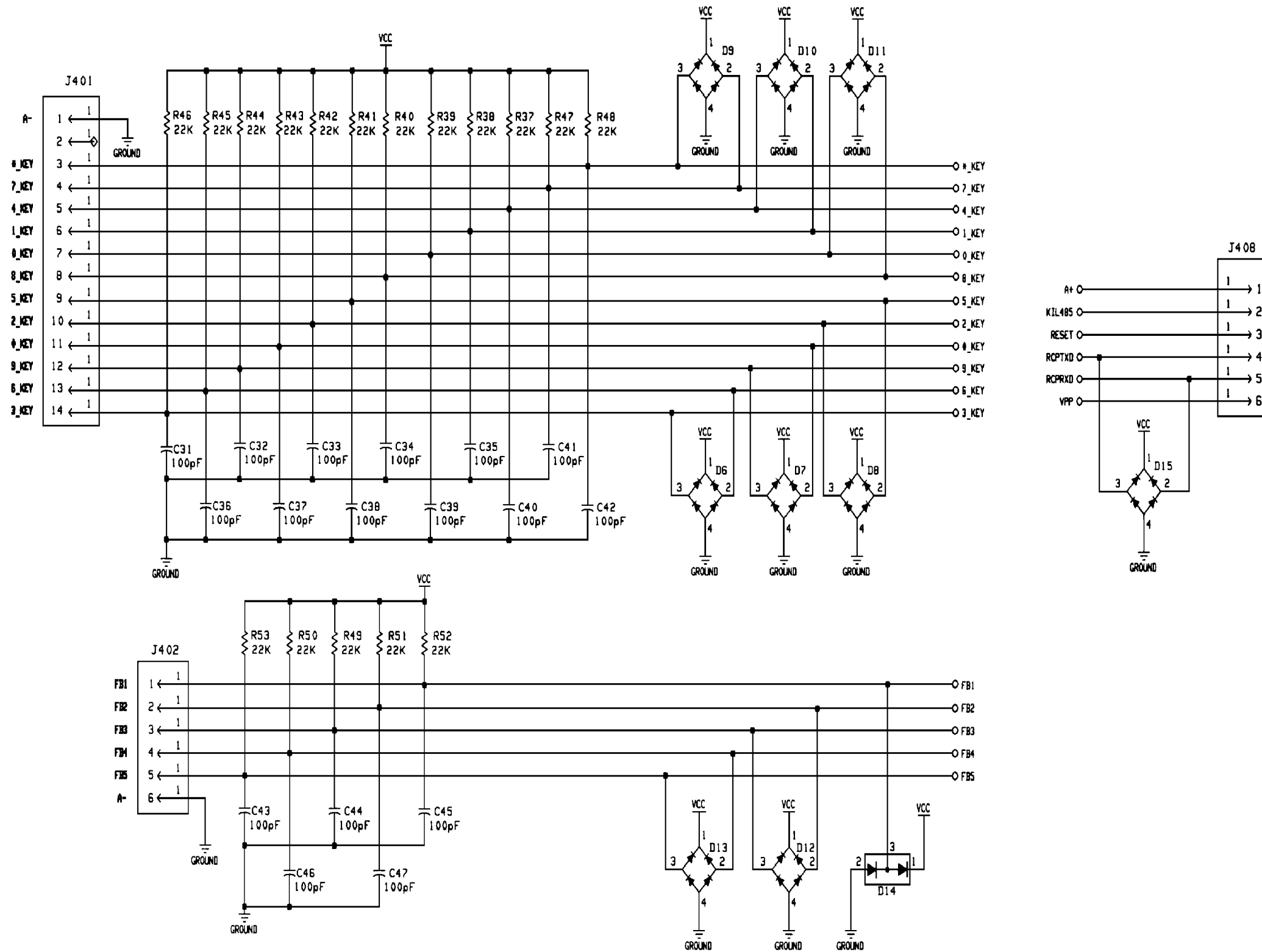
KEYPAD/FREQUENCY SELECT BOARD
188D5771G1
 (188D5772, Sh. 4, Rev. 1)



DESKTOP INTERCONNECT BOARD CONNECTORS

KEYPAD/FREQUENCY SELECT BOARD
188D5771G1
(188D5772, Sh. 5, Rev. 1)

SCHEMATIC DIAGRAM



KEYPAD/FREQUENCY SELECT BOARD

188D5771G1
(188D5772, Sh. 6, Rev. 1)

9. REPLACEABLE PARTS

Replaceable assemblies can be ordered through M/A-COM Service Parts. Component items listed in the following parts lists and identified with M/A-COM part numbers are available through M/A-COM Service Parts. All other components are for reference only and are considered common parts. These items can usually be obtained from your local electronic parts distributor.

To order replacement parts, call or FAX our on-line ordering system:

North America: 800-368-3277
 FAX: 800-833-7592
 e-mail: customerfocus@tycoelectronics.com
 International: 434-455-9217 (Latin America, Asia Pacific)
 434-455-9219 (Europe, MiddleEast, Canada)
 FAX: 434-455-6685
 e-mail: InternationalCustomerFocus@tycoelectronics.com

Sym.	Part No.	Description
CAPACITORS		
C1 & C2	19A702061P61	Ceramic: 100 pF $\pm 5\%$, 50 VDCW, temp coef 0 ± 30 PPM.
C3 & C4	19A702061P29	Ceramic 22pF $\pm 5\%$, 50 VDCW, temp coef 0 ± 30 PPM
C5	19A703314P10	Electrolytic: 10 uF -10+50%, 50 VDCW; sim to Panasonic LS Series
C6	19A701534P5	Tantalum: 2.2 uF, $\pm 20\%$, 35 VDCW.
C7	19A701534P8	Tantalum: 22 uF $\pm 20\%$, 16 VDCW.
C8	19A702052P26	Ceramic: 0.1uF $\pm 10\%$, 50 VDCW
C13 thru C47	19A702061P61	Ceramic: 100 pF $\pm 5\%$, 50 VDCW, temp coef 0 ± 30 PPM.
DIODES		
D1	19A700083P108	Silicon, Zener: 15 Volt; sim to BZX84-C15
D2 & D3	19A149615P1	Silicon: Diode Bridge; sim to BGX50A
D4 & D5	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99
D6 thru D13	19A149615P1	Silicon: Diode Bridge; sim to BGX50A
D14	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99
D15	19A149615P1	Silicon: Diode Bridge; sim to BGX50A
JACKS		
J401 thru J404	19A703248P11	Post: Gold Plated, 10 mm length.
J406 thru J408	19A703248P11	Post: Gold Plated, 10 mm length.

Sym.	Part No.	Description
PLUGS		
P207 & P208	19A704779P11	Connector; sim to Molex 22-17-2122.
P403 & P404	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P406	19A702104P2	Connector: Shorting Jumper, Gold Plated.
TRANSISTORS		
Q1 thru Q5	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
RESISTORS		
R1	19B800607P105	Metal film: 1M ohms $\pm 5\%$, 1/8 w.
R2 & R3	19B800607P101	Metal film: 100 ohms $\pm 5\%$, 1/8 w.
R4 & R5	19B800607P472	Metal film: 4.7K ohms $\pm 5\%$, 1/8 w.
R6	19B800607P102	Metal film: 1K ohms $\pm 5\%$, 1/8 w.
R7	19B800607P103	Metal film: 10K ohms $\pm 5\%$, 1/8 w.
R8	19B800607P223	Metal film: 22K ohms $\pm 5\%$, 1/8 w.
R9	19A702931P301	Metal film: 10K ohms $\pm 1\%$, 200 VDCW, 1/8 w
R10	19B800607P103	Metal film: 10K ohms $\pm 5\%$, 1/8 w.
R11	19B800607P223	Metal film: 22K ohms $\pm 5\%$, 1/8 w.
R12 & R13	19B800607P103	Metal film: 10K ohms $\pm 5\%$, 1/8 w.
R14	19B800607P472	Metal film: 4.7K ohms $\pm 5\%$, 1/8 w.
R16	REP645621/47	Metal film: 4.7K ohms $\pm 1\%$, 1/8 w.
R17	19B800607P1	Metal film: Jumper.
R19 thru R21	19B800607P223	Metal film: 22K ohms $\pm 5\%$, 1/8 w.

Sym.	Part No.	Description
R22 thru R36	19B800607P101	Metal film: 100 ohms $\pm 5\%$, 1/8 w.
R37 thru R53	19B800607P223	Metal film: 22K ohms $\pm 5\%$, 1/8 w.
R54	19A702931P301	Metal film: 10K ohms $\pm 1\%$, 200 VDCW, 1/8 w
R55 thru R57	19B800607P223	Metal film: 22K ohms $\pm 5\%$, 1/8 w.
R58 & R59	19B800607P103	Metal film: 10K ohms $\pm 5\%$, 1/8 w.
INTEGRATED CIRCUITS		
U1	344A4707P2	Microprocessor.
U2	19A703483P304	Digital: Hex Inverter; sim to 74HC04.
U3	19A704970P1	Linear: 5 Volt Regulator with Reset Output; sim
U4	19A705980P101	Transceiver, differential Bus; sim to SN751768.
U5 & U6	19A703483P319	Digital: 4-Bit Magnitude Comparator; sim to 74HC85.
U7 & U8	19A703483P311	Digital: CMOS Quad 2-Input OR Gate; sim to 74HC32.
U9	RYT1196005/4C	RAM: 32K x 8 bit.
U10	RYT1186036/2C	EPROM, 1 MB, 128K x 8 bit.
CRYSTALS		
Y1	19A702511G70	Crystal unit, quartz.

